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TITLE: Method and system for system performance optimization via heuristically optimized buses

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CLAIMS:

What is claimed is:

1. A method for enhancing performance of a bus in a data processing system, comprising: monitoring data flow through an adapter coupled to the bus in a data processing system; determining if increased bus performance is desirable; and handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable.

2. The method of claim 1, further comprising: determining the performance by examining prior throughput of data of the adapter.

3. The method of claim 1, further comprising: changing, in small incremental steps, hardware settings upstream to the adapter; and after an optimum performance point is achieved, maintaining current state.

4. The method of claim 1, further comprising: determining whether the performance is a function of an external device connected to the adapter.

5. The method of claim 1, further comprising: reaching a decision based upon prior performance parameters of other devices coupled to the bus.

6. The method of claim 1, further comprising: determining a priority of a set of adapters, including the adapter, coupled to the bus.

7. The method of claim 6, further comprising: changing the priority throughput of at least one of the set of adapters.

8. The method of claim 1, further comprising: simultaneously monitoring throughput of the adapter.

9. A system for optimizing the performance of a bus, comprising: a first bus coupled to at least one central processing unit (CPU) having a code module embedded therein; at least one input/output (I/O) adapter coupled to the first bus; a driver for the at least one input/output (I/O) adapter residing in the at least one central processing unit (CPU); and a bus monitor coupled to a hardware bus control unit residing in the code module wherein information acquired by the bus monitor is processed, and a decision is made to increase adapter throughput.

10. The system of claim 9, further comprising a second bus disposed to be monitored by the bus monitor, and connected to the at least one input/output (I/O) adapter.

11. The system of claim 9, wherein the code module comprises: a performance optimizer unit, wherein a process management queue is scanned, a determination as to weather the process management queue have a high priority I/O process; a process management unit coupled to the performance optimizer unit; and a hardware bus control unit, wherein bus performance is being read, coupled to the performance optimizer unit.

12. The system of claim 11, further comprising device driver, wherein at least one bus parameter in the I/O adapter is changed, coupled to the process management unit.

13. The system of claim 11, wherein the hardware bus control unit changes at least one bus parameter.

14. The system of claim 9, wherein the hardware bus control unit is coupled to an I/O bus hub.

15. A code module for heuristic bus optimization, comprising: a performance optimizer unit; a hardware bus control unit coupled to the performance optimizer unit; and a process management unit managing at least one device driver.

16. The code module of claim 15, wherein the performance optimizer unit scans a process management queue and determines whether the process management queue includes a high priority I/O process.

17. The code module of claim 15, wherein the performance optimizer unit queries the hardware bus control unit for bus performance of I/O devices.

18. The code module of claim 15, wherein the performance optimizer unit determines whether bus performance is maximized for the most critical I/O process.

19. The code module of claim 15, wherein the performance optimizer unit passes at least one parameter to the hardware bus control unit and the at least one device driver.

20. The code module of claim 15, wherein the hardware bus control unit reads bus performance.

21. The code module of claim 15, wherein the at least one device driver changes at least one bus parameter in an I/O adapter.

22. The code module of claim 15, wherein the hardware bus control unit changes at least one bus parameter in an I/O bus hub.